Fig. 1

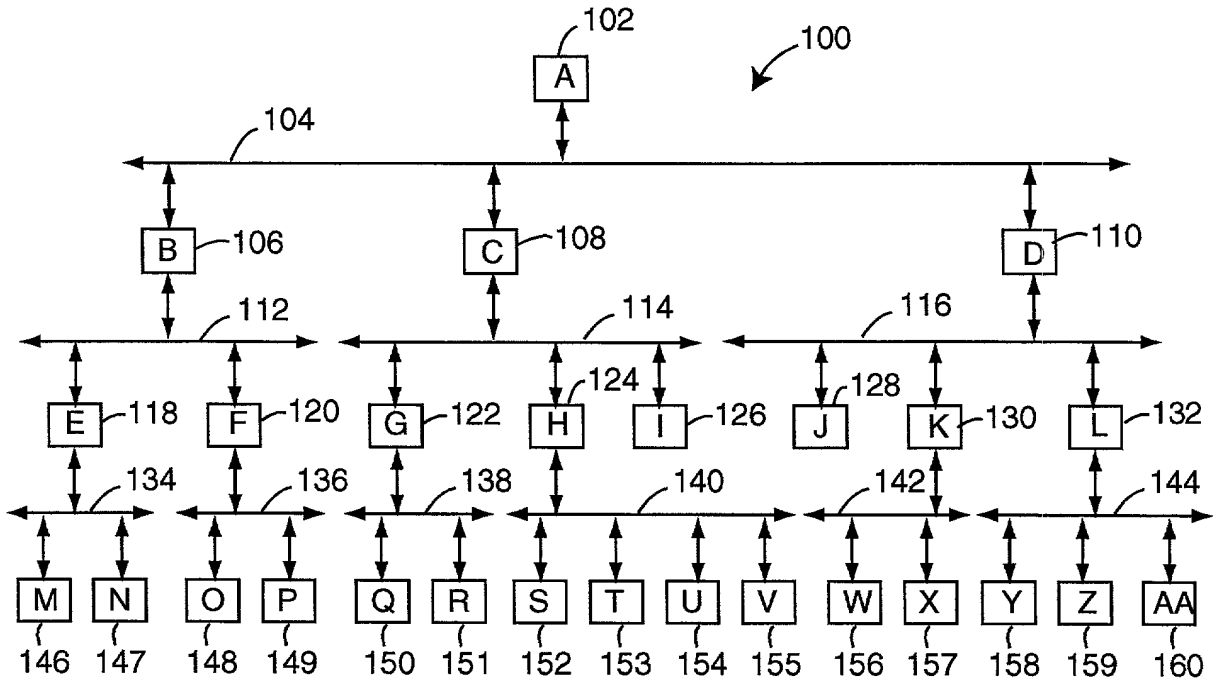

100
102
A
104
B
106
C
108
D
110
112
114
116
E
118
F
120
G
122
H
124
I
126
J
128
K
130
L
132
134
136
138
140
142
144
M
N
O
P
Q
R
S
T
U
V
W
X
Y
Z
AA
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160

Fig. 2

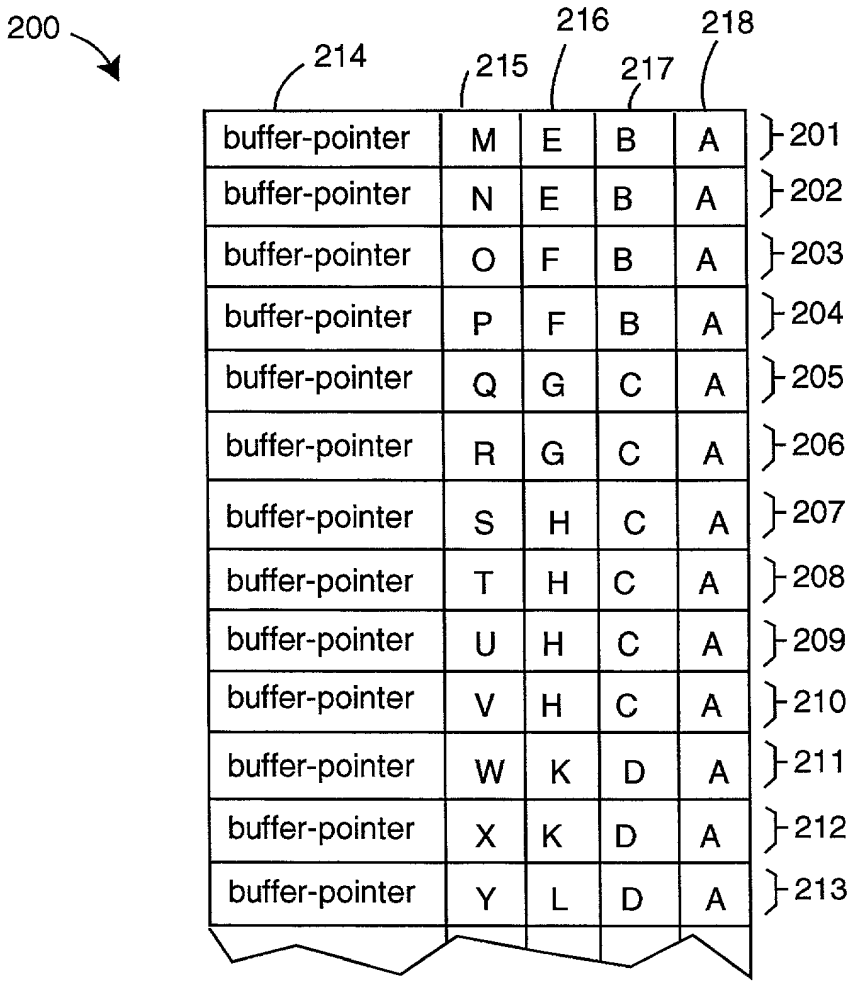
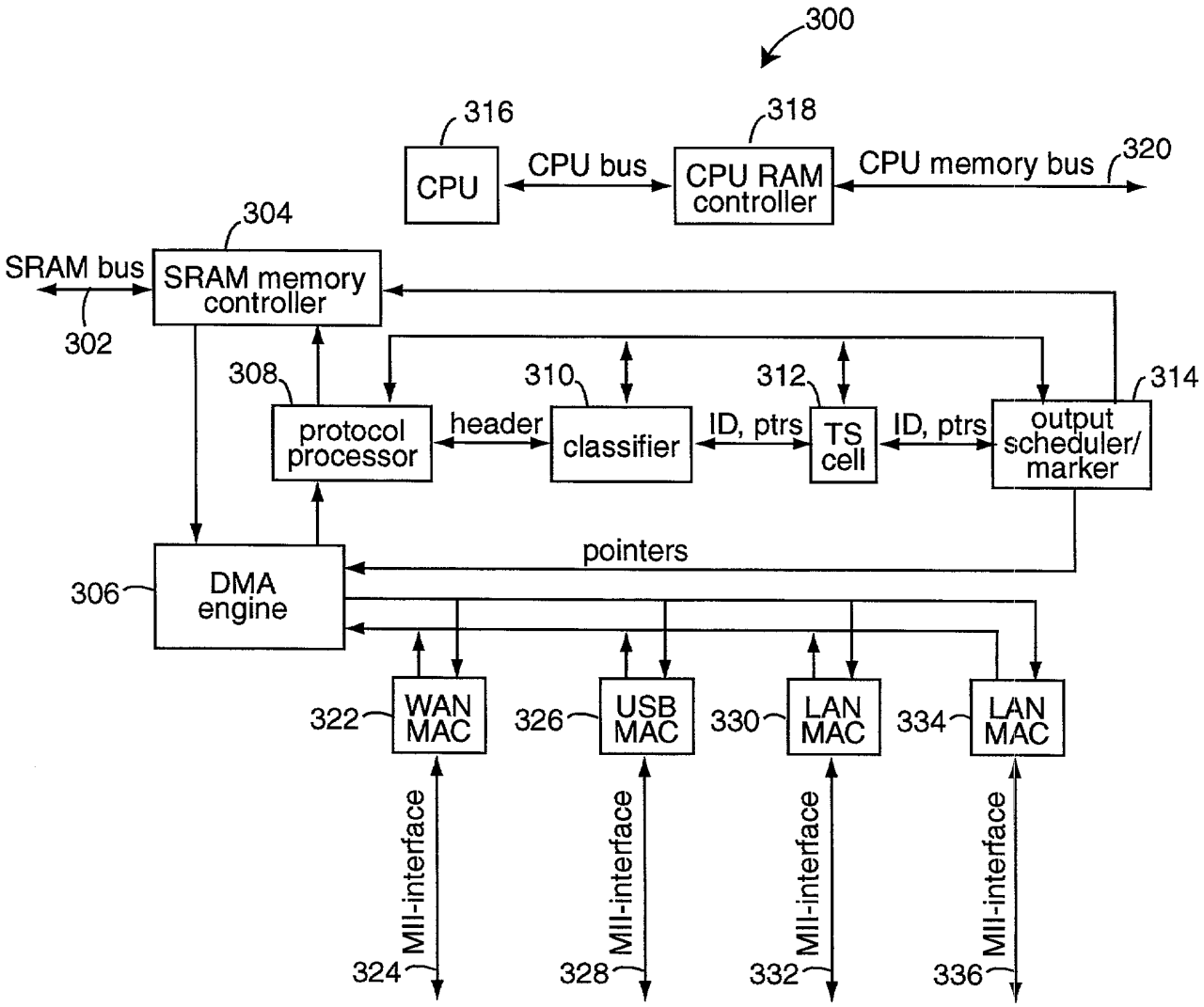

200
214
215
216
217
218
buffer-pointer M E B A 201
buffer-pointer N E B A 202
buffer-pointer O F B A 203
buffer-pointer P F B A 204
buffer-pointer Q G C A 205
buffer-pointer R G C A 206
buffer-pointer S H C A 207
buffer-pointer T H C A 208
buffer-pointer U H C A 209
buffer-pointer V H C A 210
buffer-pointer W K D A 211
buffer-pointer X K D A 212
buffer-pointer Y L D A 213

Fig. 3


300
316
318
CPU
CPU bus
CPU RAM controller
CPU memory bus
320
304
SRAM bus
SRAM memory controller
302
308
310
312
314
protocol processor
header
classifier
ID, ptrs
TS cell
ID, ptrs
output scheduler/ marker
pointers
306
DMA engine
322
WAN MAC
326
USB MAC
330
LAN MAC
334
LAN MAC
MII-interface
MII-interface
MII-interface
MII-interface
324
328
332
336

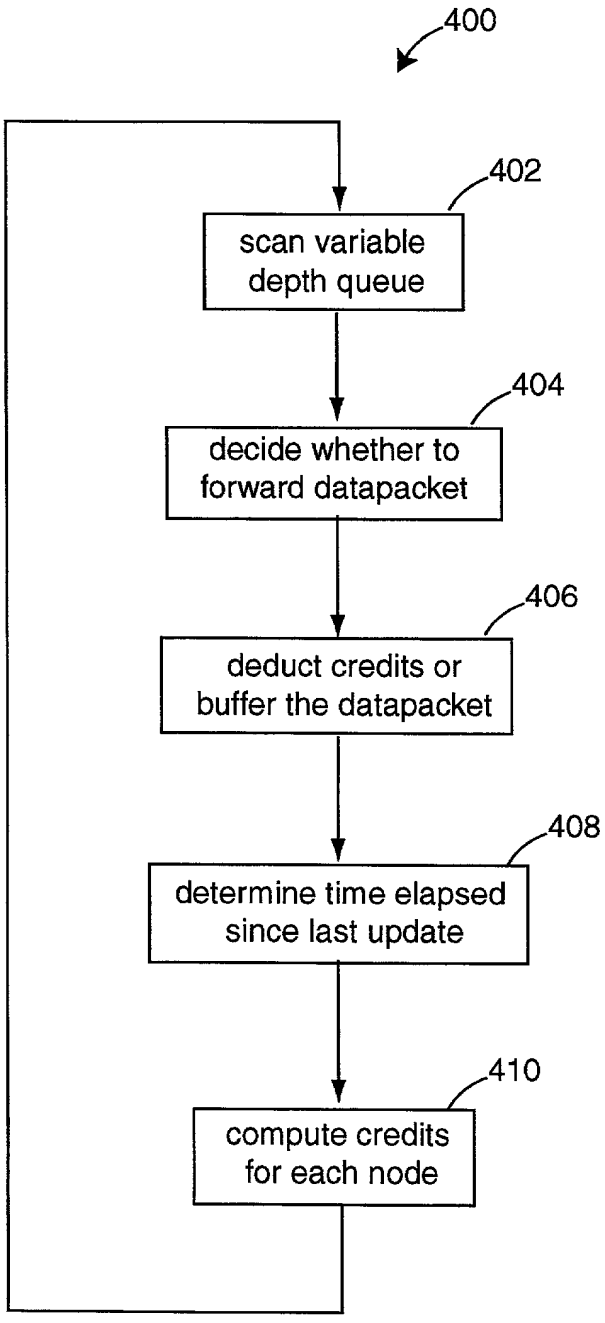

400
402
scan variable depth queue
404
decide whether to forward datapacket
406
deduct credits or buffer the datapacket
408
determine time elapsed since last update
410
compute credits for each node

Fig. 4